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A 5- GHz CMOS Low Noise Amplifier with High Gain and Low Power using Pre-distortion Technique

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Abstract: In this paper, a linearization technique called Pre-distortion is proposed with low noise amplifier and the design was implemented in 90-nm CMOS process .In this proposed design, pre-distortion circuit is employed in front of the low noise amplifier, which comprises of current reuse structure with source follower at the feedback reduces the power dissipation at the transmitter side of the amplifier. Pre-distorter line arizer improves the overall power efficiency of the LNA, with which high gain and low power is achieved. This proposed architecture supports the frequency of 5-GHz suitable for multiband standards with the wireless receivers applications. At 5-GHZ frequency it achieves high gain of 25 dB with low NF of 1.0 dB and Power gain (S_{21}) of 27.64 dB is obtained with good matching at input (S_{11}) < -10dB, which consumes low power of 5nW with efficient power at supply voltage of 3.3 V.

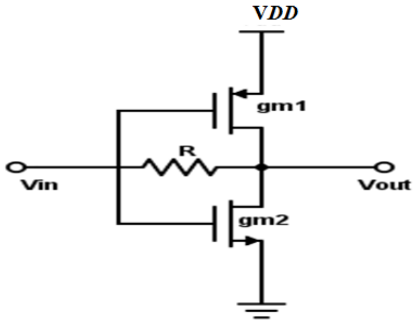
Keywords: Pre-Distortion (PD), Low Noise Amplifier (LNA), Impedance matching, Noise, Indcutorless, low power

1. INTRODUCTION

Low noise amplifier support broadband standards with the advantage of low power and it is used for multi standard wireless applications. LNA permits performance of the design with various parameters like noise figure, power efficiency, gain of the LNA and the various S-parameters of the low noise amplifier with good matching at the input side of the design. Low noise amplifier is designed and implemented in the existing architecture with inductor less design [1]. In LNA, chip cost is reduced with the help of this inductor less design. This design includes two stages with the first stage, principle of current reuse amplifier followed by the second stage of feedback principle with source follower structure and this design allows low noise with multiband frequency of operation.

In Fig 1, these two stages principles are figured. In Fig 1(a), the principle of current reuse stage with parallel arrangement of Nmos and Pmos transistors with feedback resistors. This structure provides high gain with effective transconductance. The main advantage of current reuse structure [2] is that efficiency of current in the LNA is improved effectively with low power and noise with which high gain and impedance is obtained at the output of the amplifier. In Fig 1(b), the source follower stage with active feedback is shown. This structure allows higher trans conductance with higher efficiency of power. This active feedback supports wideband performance with input matching [3].With the advantage of less complexity, the active feedback function as amplifier of trans impedance so that design of inductorless low noise amplifier is created. The main objective of this feedback principle is to achieve high gain with efficient power consumption.

In Fig 1(c), The combination of current reuse structure with source follower at the feedback is integrated and this allows higher transconductance simultaneously with less power. With this combined architecture, the extension of bandwidth is realized with improved performance of the LNA.



(a)

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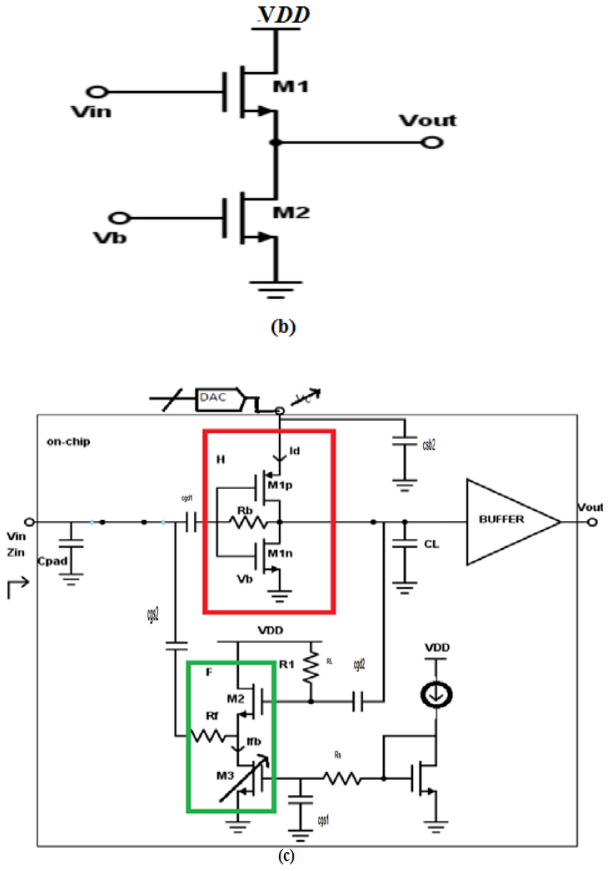

Figure 1. LNA design: (a) Current reuse structure, (b) source follower, (c) LNA with two transconductances amplifier

The LNA with inductor less design reduce the chip area with the result of greater accuracy. As a result of low complexity the effect of parasitics diminished and allow multiband operation. The two stages of LNA are integrated with capacitances and resistances that are parasitic in nature is used to achieve input impedance with real characteristics at the LNA's output in the feedback loop. The good input matching is achieved with high power gain and lower supply voltage [4] and that stages of LNA are suitable for UWB applications. The cascade stages does not support wideband matching, so to overcome this problem the voltage buffer is introduced to achieve low power and input matching.

In this architecture of LNA, a principle of derivative superposition is addressed with the complementary stages of the amplifier. By this method of derivative superposition [5], weak non-linear transitions is characterized and observed at input of the LNA. This principle supports wide range of operation but due to higher voltage bias it consumes high power.

This principle is mainly based on technique of Feed forward. This technique follows a principle in different regions with the implementation of transistors with the amplifiers. In this the second order amplifier of transconductance is maximized and narrow of third order transconductance effect with good wideband operation. This complementary stage involves in enhancement of transconductance [6,7] for tradeoff with good performance and low power. The feedback principle provide higher transconductance with high gain. This enhancement of transconductance are mainly achieved by inductorless design with low power.

The following sections are featured as follows. Section II describes the proposed design of LNA with pre- distortion technique. Section III will report the analysis of various parameters of LNA. The Final section IV describes the conclusion of the paper.

2. PROPOSED DESIGN

A. Basic Objective

The proposed design of pre-distortion technique with the LNA is shown in Fig. 2. This design comprises of two stages with pre-distortion circuit. In first stage of LNA, it has the stacked transistors of Nmos (M1p) and Pmos (M1n) with bias resistor RB. The complementary stages form current reuse amplifier, in which bias current is reused [8] with efficient power consumption and this principle of current reuse boosts the transconductance of LNA [9].By employing this principle, high impedance matching at the input of the LNA is attained easily. This stage of LNA achieves high gain with less noise at the output of the circuit.

In second stage of LNA, it employs principle of active feedback with source follower consisting of two Nmos M2 and M3 and feedback resistor RF. By employing this principle, overall circuit is stable and wideband matching is obtained at the input stage of the LNA. RF provide less noise. Input impedance is controlled independently by the gm of source follower stage. But this stage of feedback consumes high power. The third stage, pre-distortion [10] circuit is proposed design inserted at the transmitter side of the two stage LNA.

This pre-distortion technique contributes the main advantage of high gain with low power efficiency. Pre-

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distortion structure consists of auxillary resistor RA with parallel capacitor CP and with added resistors R1 and R2 and inductorless design [11] is used with the existing design of current reuse and source follower with feedback stage to overcome the problem of higher power consumption and to improve overall power efficiency with low noise and high gain at high frequency.

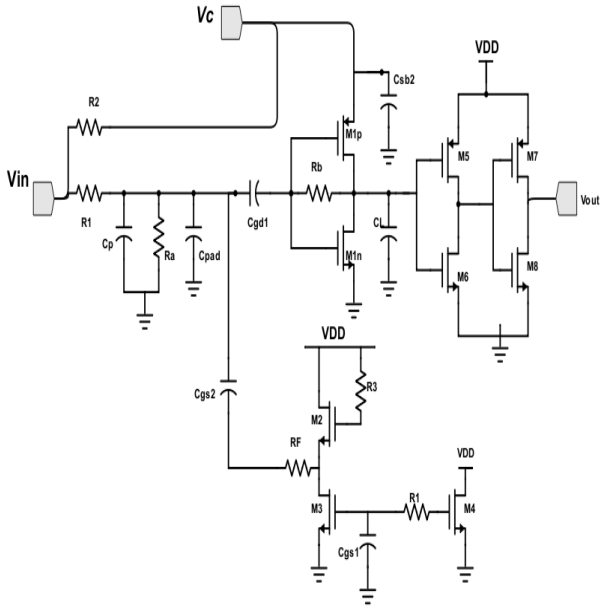

Figure 2. Proposed design of LNA with Pre-distortion

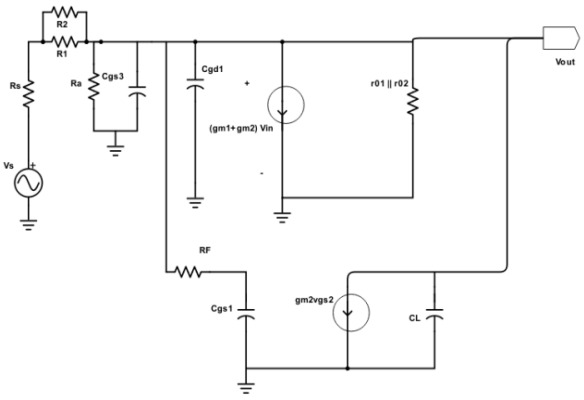

Figure 3. Proposed design: small signal equivalent circuit

The voltage gain of the first stage current reuse amplifier is given w.r.t to source resistance as

$$A_x = -\left(g_{m1} + g_{m2} - {}^{1}/_{R_f}\right).(R_s \| r_{01} \| r_{02}) \quad (1)$$

The transconductance and output resistance (R_0) of first stage given by

$$G_m = G_{m1} + G_{m2}, \text{R0}=(R_s \| r_{01} \| r_{02}) \quad (2)$$

$$A_x = -\left(G_{m1} - {}^{1}/_{R_f}\right).(R_0) \quad (3)$$

The voltage gain of second stage with high frequency is given by

$$A_y = \frac{(g_{m1} + sC_{gd1})(G_s + s\,C_s)}{\begin{matrix} S^2[(C_s + C_{gs1})(C_0 + C_{gd1}) + C_sC_{gd1}] + \\ s[(C_s + C_{gs1})(G_0 + g_{m1}) + G_0C_{gd1} + \\ [(C_0 + C_{gd1})G_s] + (G_0 + G_{m1})G_s \end{matrix}} \quad (4)$$

The overall voltage gain of proposed LNA design with pre-distortion is expressed in (5)

$$A_v = \left| \begin{matrix} \frac{(g_{m1}+sC_{gd1})(G_s+s\,C_s)}{S^2[(C_s+C_{gs1})(C_0+C_{gd1})+C_sC_{gd1}]+ \\ s[(C_s+C_{gs1})(G_0+g_{m1})+G_0C_{gd1}+ \\ [(C_0+C_{gd1})G_s]+(G_0+G_{m1})G_s \\ -\left(G_{m1} - {}^{1}/_{R_f}\right).(R_0) \end{matrix} \right| \cdot \left| \left(\frac{1}{S_{cgs3}} \| Ra\right) + (R1 \| R2) \right| \quad (5)$$

In this proposed design the overall gain obtained in (5) is high at high frequency and consumes low power with excellent efficiency at the output of the design. The main performance parameters of LNA is gain which is achieved with good quality with wideband input matching at 5-GHz frequency. The gain obtained in the proposed with higher gm [12] and this parameter reduce the power consumption with reduced noise.

B. Input Matching

In this proposed design both the stages of amplifier contributes high input matching, so that it is well suited for multiband frequency operation. In this feedback principle mainly included to reduce the gain tradeoff and allow extended bandwidth.

The feedback resistor introduce the problem of noise and this can be avoided by combining two stages of LNA with pre-distortion circuit. So low noise is obtained with good performance of LNA. Input matching is attained easily by using feedback resistor RF and load resistor. The impedance at input of the proposed LNA design is expressed in (6).

$$Z_{in3} = Z_{in2} \| Z_{in1} \quad (6)$$

$$Z_{in2} = \frac{g_{m1}+s(C_{gs2}+C_L)+G_0}{S^2[C_{gs2}C_{gd1}+C_{gd1}C_L+C_{gs2}C_L]+S[G_0+C_{gd1}g_{m1}+C_{gs2}G_0]} \quad (7)$$

$$Z_{in1} = \frac{R_F}{1+A_v} \quad (8)$$

The RF is the feedback resistor, that introduces noise in design of LNA. This noise is controlled by inserting pre-

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distortion circuit and support high input matching with good performance.

C. Noise Figure

In LNA, the main contributions of noise is due to the feedback resistor and it result in high noise figure of the LNA design. The noise current produced by RF at the output (i.e.) short circuit is expressed in (9).

$$\overline{i^2 R_f} = \frac{4KT\Delta f}{R_f} \quad (9)$$

The noise contributed due to the MOS transistors in the LNA design is given in (10).

$$\overline{i^{2M_0}} = 4KT\Delta f\, \gamma_0 g_{d0} \quad (10)$$

The noise results of this LNA design is increased noise figure with distortions in the design output of LNA. To overcome this drawback in LNA the pre-distortion circuit is proposed with LNA by inserting the pre-distortion circuit.

In LNA design, the contribution of noise by MOS transistor and resistors are completely solved by this pre-distortion at the input of the LNA with lowered noise at output of the design. In proposed design, there is noise factor due to auxillary resistor with the added resistors at input of the design. But this noise factor is totally compensated by adding the feedback capacitor in parallel with the auxillary resistor Ra and noise is cancelled with low noise and high gain. The noise factor of the proposed circuit includes nR1, nR2, nRa with source resistor and feedback resistor is expressed in (14).

$$\overline{V^2_{out,nR1}} = \frac{4KT\Delta f}{R1} \cdot \frac{Rs^2 gm2^2}{(g_{m2}R_a+1)^2} \quad (11)$$

$$\overline{V^2_{out,nR2}} = \frac{4KT\Delta f}{R2} \cdot \frac{Rs^2 gm2^2}{(1+gm_2R_a)^2} \quad (12)$$

$$\overline{V^{2}_{out,nRa}} = 4KT\Delta f R_a . Rs^2 . \frac{gm2^2}{(1+gm_2Ra)^2} \quad (13)$$

$$NF = 1 + \frac{R_a}{R_s}.\frac{1}{Av^2} + \frac{R_s}{R_1}\left[1 - \frac{R_a}{R_s|A_v|}\right]^2 + \frac{R_s}{R_2}\left[1 - \frac{R_a}{R_s|A_v|}\right]^2 \quad (14)$$

In this Av is the voltage gain that is greater than unity and this condition is applied to above equation and total noise factor is obtained. In proposed design, the capacitor added at the feedback boosts the transconductance [12] of LNA as a result noise figure is lowered at high frequency.

3. SIMULATION RESULTS

The low noise amplifier was proposed with pre-distortion Circuit. This circuit was implemented and designed in CMOS technology of 90-nm using Cadence Virtuoso the results are simulated and measured. The parametric values used in the circuit are tabulated in Table 1.

Table 1. Parametric Values of LNA Circuit

Parameter	Value	Parameter	Value
$(W/L)_{M1p}$	4µm/100nm	R_1	$22k\Omega$
$(W/L)_{M1n}$	$2\mu m/100nm$	R_2	1 $k\Omega$
$(W/L)_{M2}$	$120nm/100nm$	R_3	1 $k\Omega$
$(W/L)_{M3}$	$120nm/100nm$	R_F	1 $k\Omega$
$(W/L)_{M4}$	$120nm/100nm$	R_s	1 $k\Omega$
$(W/L)_{M5}$	4µm/100nm	R_a	70 Ω
$(W/L)_{M6}$	$2\mu m/100nm$	C_p	47 nF
$(W/L)_{M7}$	4µm/100nm	C_L	500 fF
$(W/L)_{M8}$	$2\mu m/100nm$	C_{pad}	1 pF
C_{gs1}	1 pF	C_{gs2}	10 pF
C_{sb2}	1 pF	C_{gd1}	10 pF

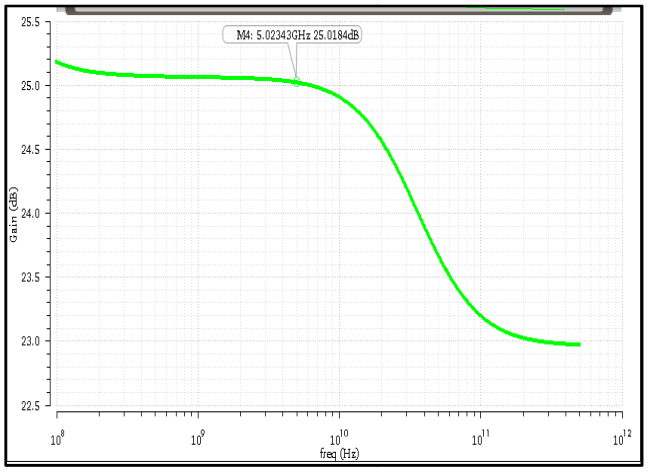

Figure 4. Gain of proposed pre-distortion circuit with LNA

The analysis of gain for proposed LNA is shown in Fig 4. In this low noise amplifier, the feedback resistors provide small gain with reduced output impedance that is the feedback principle has the major drawback of less gain (i.e.<unity). By introducing the technique of Pre-distortion

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with LNA result in high gain of 25 db. This result of high gain is achieved at 5-GHz frequency.

The proposed circuit consumes low power and its simulation results are plotted in Fig.5.This pre-distortion circuit when inserted in front of the low noise amplifier achieves good power efficiency. The total consumption of power of the proposed design of the overall circuit is 5nW at supply voltage of 3.3 V and so it suitable for many low power application with high gain.

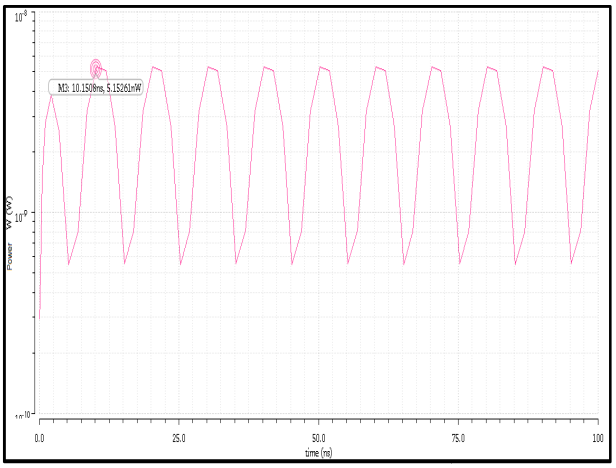

Figure 5. Power analysis of the Proposed design

The performance parameters of the LNA are figured in the basis of noise figure. The result of Noise figure is shown in Fig. 6. The feedback principle of LNA provides low NF with the resistor at the feedback and this low NF result in higher voltage gain of the LNA design. The Noise figure of 1.0 dB with increased frequency of 5-GHz.

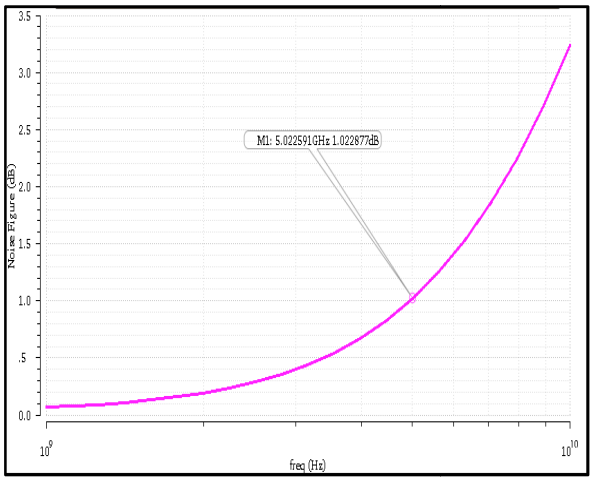

Figure 6. Noise Figure of the pre-distortion design

The input matching of the design is shown in Fig. 7. It achieves wide input matching due to the feedback loop of the LNA. The input matching is improved by this design with S(1,1) less than -10 db at 5-GHz frequency. The input is isolated from the node by this improved input matching.

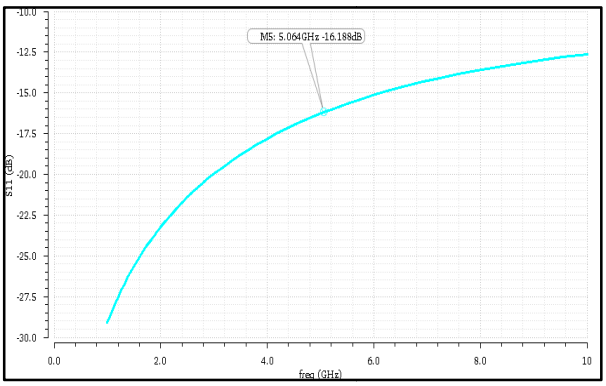

Figure 7. S(1,1) Reflection coefficient at input of proposed Design

The S(2,2) reflection coefficient at the output of the proposed design is < -10 dB at 5-GHz frequency is figured in Fig. 8 . This provides return loss at the output of the circuit and the plotted S(2,2) of the design results in the value of -16.087 dB.

The proposed design with Pre-distortion circuit at the transmitter side of the low noise amplifier provide high forward gain S(2,1) of 27.64 dB and reverse transmission S(1,2) of -60.754 dB and these results are figured in Fig. 9 and Fig. 10. The Pre-distortion technique employed with the result of higher gain at 5-GHz frequency and this higher gain allows good performance of the LNA.

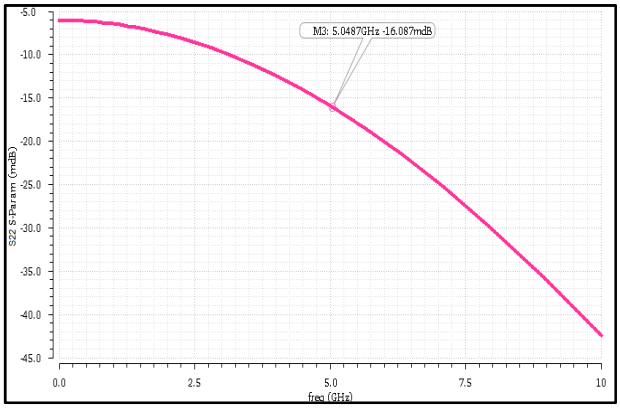

Figure 8. S(2,2) Reflection coefficient at the output of the LNA

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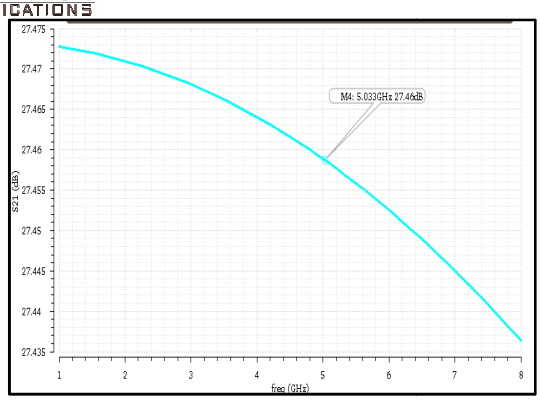

Figure 9. S(2,1) Forward gain of the Proposed design

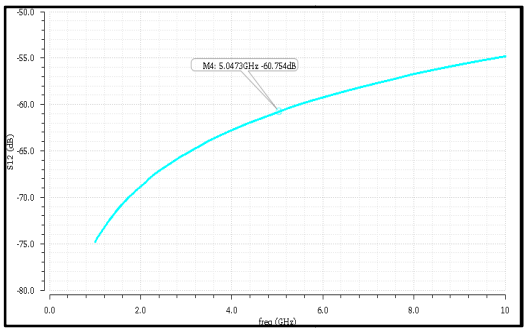

Figure 10. S(1,2) Reverse transmission of the Pre-distortion Design

The Performance parameters of proposed structure like gain, power, Noise figure, various S-parameters are compared with the previous design of LNA and tabulated in Table2.

Table 2. Comparison of performance parameters of pre-distortion design with recent works

Ref	[1]	[2]	[4]	[9]	[12]	This work					
Technology (nm)	130	180	90	130	110	90	5	25	1.0	< -10	27.64
Frequency (GHz)	0.1-2.1	3-12	3.1-10.6	3-5	3-10	5	5	25	1.0	< -10	27.64
Gain (dB)	21.2	20.24	20	13	18	25					
NF (dB)	2.0	1.72-1.99	1.2-2.6	3.5-4.5	2.4-2.9	1.0					
S_{11} (dB)	-	<-10	<-10	<-8	<-10.7	<-10					
S_{21} (dB)	-	19.24-20.24	≥20	13	17.5-18.7	27.64					
Power (mW)	7.05	23	12.6	3.4	8.30	5(n)					
Supply (VDD)	1.3	1.8	0.6	1	1.2	3.3					

4. CONCLUSION

This paper describes the design of the Pre-distortion circuit with the low noise amplifier to achieve excellent efficiency of power and this employed proposed technique support high frequency of 5-GHz with increased gain and the overall design of LNA with Pre-distortion consumes low power with good matching at input. The results are simulated in 90-nm technology and measured at 5-GHz frequency. The simulated analysis shows high gain of 25 dB with NF 1.0 dB and S_{21} of 27.64 dB with impedance matching at input S_{11}<-10 dB and it consumes power of 5nW at 3.3 V power supply with good performance and it is well suited for many multiband receiver applications.

REFERENCES

[1] Marcelo De Souza, Andre Mariano and Thierry Taris , " Reconfigurable Inductorless Wideband CMOS LNA For Wireless communications" IEEE transactions on circuits and systems–I: regular papers, vol. 64, no. 3, March 2017.

[2] MohsenHayati, SajadCheraghaliei , SepehrZarghami ,"Design of UWB low noise amplifier using noise canceling and Current reused techniques" Integration the VLSI journal 60 2018 232–239.

[3] Mahdi Parvizi, KarimAllidina and Mourad N. El-Gamal, "An Ultra-Low-Power Wideband Inductorless CMOS LNA With Tunable Active Shunt-Feedback" IEEE transactions on microwave theory and techniques : vol. 64, June 2016.

[4] Sunil Pandey; Jawar Singh, "A 0.6 V, low-power and high-gain ultra wide band low-noise amplifier with forward body-bias technique for low-voltage operations" IET Microwaves, Antennas & Propagation : volume : 9 , 2015.

[5] Wei Gao, Zhiming Chen, Zicheng Liu, Wei Cui, XiaoyanGui "A Highly Linear Low Noise Amplifier With Wide Range Derivative Superposition Method" IEEE microwave and wireless components letters, vol. 25, no. 12, December 2015.

[6] Zhijian Pan, Chuan Qin, Zuochang Ye, Yan Wang, "A Low Power Inductorless Wideband LNA With Gm Enhancement and Noise Cancellation" IEEE Transactions on Circuits and Systems I: regular Papers, vol: 65, 2018.

[7] Zhijian Pan, Chuan Qin, Zuochang Ye, Yan Wang, Zhiping Yu, "Wideband Inductorless Low-Power LNAs with Gm Enhancement and Noise-Cancellation" IEEE transactions on circuits and systems–I: regular papers , vol:65, 2018.

[8] Mahdi Parvizi, KarimAllidina, Mourad N. El-Gamal," Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 μW 0.6–4.2 GHz Current-Reuse CMOS LNA" IEEE Journal of solid state circuits : volume : 51, 2016.

[9] S.M.RezaulHasan, Muhammad Khurram,"A 3–5 GHz Current-Reuse g_m boosted CG LNA for Ultra wideband in 130 nm CMOS " IEEE transactions on very large scale integration systems, vol: 20, no. 3, March 2012.

[10] RoyaJafarnejad, AbumoslemJannesari, JafarSobhi, "Pre-distortion technique to improve linearity of low noise amplifier" .Microelectronics Journal 61 (2017).

[11] Yiming Yu, Kai Kang, Yiming Fan, ChenxiZhao, Huihua Liu, Yunqiuwu, Yong-Ling ban, Wen-Yan Yin, "Analysis and Design of Inductorless Wideband Low-Noise Amplifier With Noise Cancellation Technique" IEEE Access, vol: 5, 2017.

[12] Muyeon Lee, Ickjin Kwon, "3–10 GHz noise-cancelling CMOS LNA using gm-boosting technique", IET circuits, Devices and Systems, vol: 12, 2018.

