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Systematic Review on Multiply and Accumulate Unit (MAC) Architectures and Comparison with Various Multipliers

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ABSTRACT

The basic architecture of digital signal processing and digital image processing systems is the Multiply and Accumulate (Mac) architecture. Digital signal processing applications require Mac hardware with high speed and low power consumption as the main functions of DSPs, such as filtering and conversion, are used continuously. Macs also have applications for hardware and software. Floating-point arithmetic using the Mac architecture is more accurate but consumes more power and more silicon space. ieee-754 is a floating point algorithm that improves accuracy on Mac devices. In this systematic review, we are discussing various Mac architectures and their comparison with various multipliers.

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1. INTRODUCTION

Multiplication and scaling (MAC) is an important component in digital signal processing systems. An accumulator and a multiplier combine to create a MAC. To generate a fresh outcome that is stored in an enroll, the multiplier multiplies the samples of input that are supplied to the buffer and merges the prior and present values. Therefore, in tasks incorporating digital signal processing, both low and high capacity MACs are consistently suggested. Figure 4 illustrates a standard MAC gadget. The main functions of MAC are in filtering and convolution applications. High-precision MACs are essential in many DSP applications for the purpose to increase accuracy. MAC and floating point layout may boost the DSP system's overall performance. It is achievable to carry out MAC employing point or point coordinates. Fixed-Point Calculus In MAC, fixed-point accumulators and factors are utilized. The output's resolution diminishes when a fractional point is utilized. In this instance, the fixed point parameters were introduced into the input samples. The fixed-point sum produces the result shortly after the filter parameter and the submitted sequence are multiplied by the filter coefficient and the user-specified coefficient. The output of fixed point addition is y(n), which is the aggregate of the beforehand result and the current input. ADC measurement failure, encoding error, overflow mistakes, loop error, and cutoff error were a few of the restrictions of MAC transmissions. Division of Floating Points MAC includes floating point accumulators and multipliers. The outcome is accurately evaluated where floating point arithmetic is implemented. The multiplier accepts the input samples from the floating-point MAC. The floating-point sum receives the result of the multiplier that multiplies the input patterns. The converter generates a new output called y(n), which is preserved in a register, via combining the current input with the preceding conclusions. Despite floating-point MAC is more precise than fixed-point MAC, it demands more silicon area.

The floating-point addition operation is performed in four steps. 1. Sorting: The numbers are organized in this section from largest to smallest, or in descending order. 2. Sorting: This is the step of sorting the numbers so that their variables are equal. This process is performed by adjusting the variables of

the minor year so that the variables of the two years are equal. 3. Add or subtract: In this step, significant figures are added or subtracted from the selected numbers. remove4. Normalization: in this step, the results obtained are determined [19]. Point-of-Float Multiplier Technologies for digital signal processing and digital image manipulation relies significantly on the floating-point multiplier.

Let us assume the two floating-point numbers are m1 and m1 and the result obtained after multiplication is m, then

$m = m1*m2$

$= (-1)^{s1}.m1.2^{e1} * (-1)^{s2}.m2.2^{e2}$

$= (-1)s1+s2.p1.p2.2e1+e2$

In 1985, the IEEE released the binary floating point standard format. It consists numerous types of floating point designs, encompassing single and double exactness, rounding strategies, arithmetic operations, etc. The expression that follows can be implemented to represent the floating point number.

$Z= (-1s) *2 (exp-bias)*(1*M)$

A 32-bit floating-point integer comprises of 8 bits for the index part, 23 bits for the most significant portion, and 1 bit for the sign, in accordance with the IEEE 754 format. The subsequent standards are published in the IEEE 754 format: The first three formats use 32, 64, and 128 bits correspondingly. and have been employed for binary floating-point values. The last two forms are used for floating point binary numbers, which rely on 64 and 128 bits. [10]

Table 1. Different standards in IEEE 754 format

Name	Common name	Base	Digits	E min	E max
Binary 32	Single precision	2	23 +1	-126	+127
Binary 64	Double precision	2	52 +1	-1022	+1022
Binary 128	Quadruple precision	2	112+1	-16382	+16382
Decimal 64		10	16	-383	+383
Decimal 128		10	34	-6143	+6143

2. MAC ARCHITECTURES

Employing the input registers, the MAC's input is transmitted in one clock cycle to the multiplier block. Assuming an equal-length trigger, acquire the total period of each block. If the input is accessible then the block is active. The designed MAC device contains an energy delay product of 177.95 * 10-15J. Using block activation technology, a high-power, low-loss MAC structure is designed for DSP applications. The block chain technological-driven MAC tube architecture is portrayed in the image. The fundamental elements of quantum computing, invertible logic gates, are put to use in Vedic multipliers and MAC designs. The Vedic multiplier's main feature is its knack to compute partial items in a single step. A circuit containing primarily of flipping logic gates is non-invasive. An inverting logic Boolean algorithm refers to one in which each integer of the input signal can be allocated to an individual quantity of the outcome. Power Inverse logic and Vedic parameters coupled may yield superior MAC designs. Partial conclusions can be generated using the Urdhava sutra's problem transfer procedure. Improved unit yields lead in a substantial breakthrough in design. In optical and nanoscale applications, inverting logic gates are applied for lowering power dissipation. The Booth, Wallace, and Vedic multipliers are among the multipliers with which the MAC architecture is contrasted. Table 2 summarizes the distinct architectures' power, location, and speed.

Table 2**.** Analysis of MAC with different multipliers.

Parameter	Booth Multiplier	Both Wallace recoded tree multiplier	Vedic multiplier with Koggestone adder and reversible logic (proposed model)	Vedic multiplier and reversible logic (proposed model)
Power nw)	18398.67	17567.678	15621.12	15546.567

Speed (ns)	6.56 7	6.436	1.932	5.667
Area ($um^{2)}$	2322	2379	1972	2123

3. Guard blocks are employed in a multi-binary stacking creation that is believed to operate well on longer MAC loops. No additional processing is necessary for the reason carrier emergence in this architecture occurs in the subsequent stage of the MAC pipeline. Every second, this structure produces revenue and generates value. Admit it The pipe register, which has the equivalent length as an individual adder, is followed by a storage adder. Throughout the construction treatment, the portable tent connector is used once the final plug is removed. It has been proved that this architecture is more consistent than the conventional two-cycle MAC implementation. A product reduction item that diminishes the design's power consumption is presented in the low-power architecture that is advised. The analysis results are dedicated to MAC devices FFT and FIR calculations are faster. Many machines are used in designs that use full complements to speed up multiplication. Because the full complement is being used, more power is required to drive the signal, resulting in higher power consumption. The design was compared to the RTL cadence using the TSMC 65nm node and the results are compared to the MAC architectures in the table 3.

Table 3. Comparison of conventional MAC and the proposed MAC in ASIC domain.

Design	**8bit MAC unit**		
4:2 Compressor cell	**Using basic tree cells [8]**	**Using Full Adders**	**Proposed**
Area	1251.72	1086.12	1083.24
Delay	2.968	2.546	2.2874
Dp	77.54	63.588	63.326
Lp	12.57	13.194	9.998
Tp	90.11	76.782	73.324

A moo control and exceedingly effective floating-point MAC engineering is proposed which employments BCD squares and the yield of the MAC is additionally delivered within the BCD arrangement. Here in this design, a double to BCD converter and BCD piece are utilized. The parallel to BCD converter is utilized since the yield of the multiplier is in parallel arrange which has to be sent to the BCD square. A proficient MAC design is outlined and analyzed utilizing cadence virtuoso in 90nm innovation.

2.1. Multiplication

A fundamental purpose of the MAC unit is multiplication. Multipliers have a wide broadcast area, a substantial latency, and a high power expenditure. Digital signal processing solutions necessitate fast multipliers as a vital ingredient. Two primary conditions should be satisfied for the MAC unit to function effectively and quicker. Dipping the sum of fractional yields in the multiplication hunk is the first move, and minimizing the accumulator's burden is the second. The factor of two provides the critical path in a digital system by requiring an important quantity of delay among its basic operational blocks. This section explores the MAC considering the Booth, Conventional, and Vedic multipliers.

2.2. Vedic multiplier

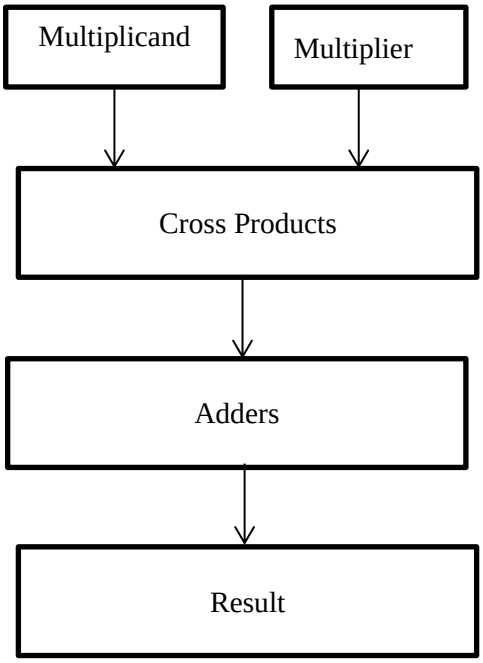

Figure 1. Construction of Vedic multiplier

The capacity to solve complex problems through simple strategies is the primary objective of Vedic mathematics. Regardless of how short the formula is, they become practically trivial to perform. Urdhva-tiryagbhyam (Steeply and slanting) sutra is widespread formulation pertinent to proliferation action. The multiplication of polynomials lays the foundation of its algebraic principle. The Vedic multiplier consuming Urdhva-tiryagbhyam sutra of breadth NXN will yield the $2N-1$ cross results of distinct dimensions which when merged forms $(\log_2 N+1)$half-done outcomes. Using the Sutra, horizontally and transversal operations obtain the partial products. As an outcome, the delay doubles the adder delay. Adding units accumulating the largest amount of bits in the cross product would constitute the critical path. All multiplier bits are always brought for consideration in the cross product is shown in Figure 1.

2.3. Booth Multiplier

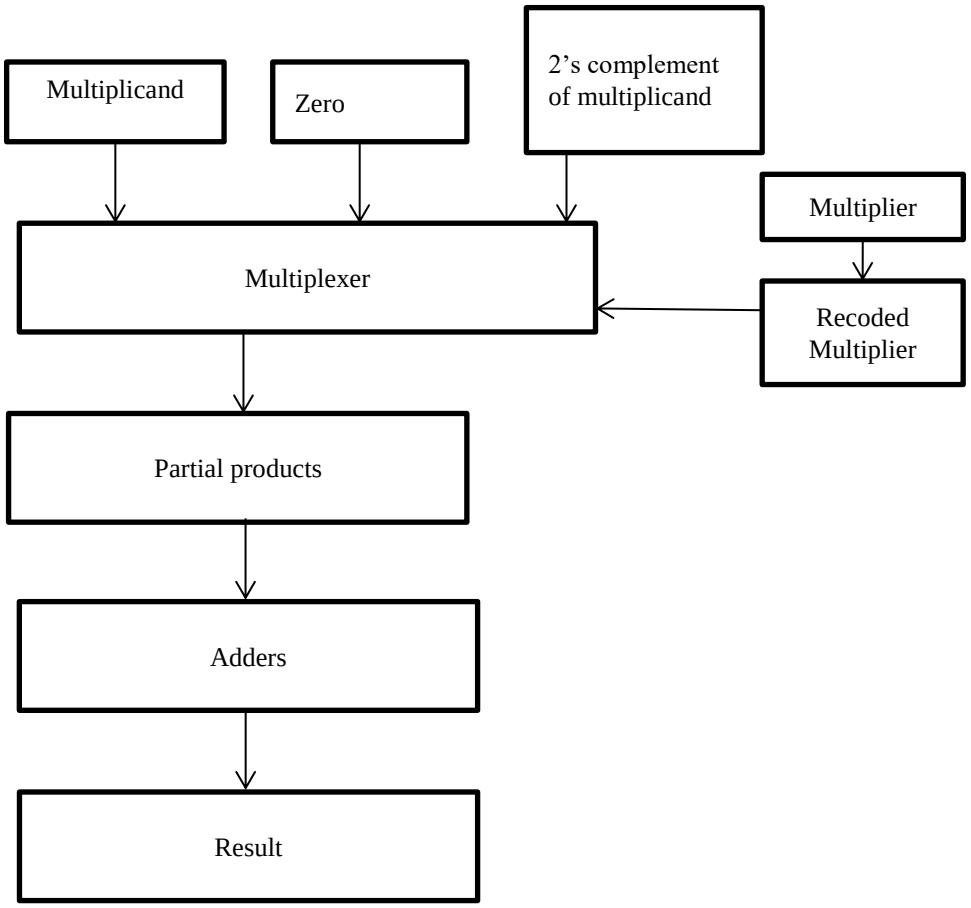

Figure 2. Block diagram of recoded multiplier

Recoded booth multiplier is another term for the booth multiplier, when the coefficient is revised in addition to its multiplier retains its value unchanged. As a recoded multiplier, the multiplicand and transformed multiplier thereafter serve to execute the multiplication. The Multiplier leverages Radix 2^r multipliers, which yields N/r partial goods, every one of which hang on r bits of the multiplier, to diminish the quantity of unfinished products in the multiplier. A smaller and faster CSA (Carry Save Adder) environment is formed when there are fewer partial yields. A radix-4 multiplier, for instance, yields $N/2$ partial products. $N/2$ partial products are produced by each radix-4 multiplier. According to two bits of Y, each partial product may represent 0, Z, 2Z, or 3Z. Although 3Z is a hard multiple that demands a slow carry-propagate insertion of $Z + 2Z$ before partial manufacturing begins, evaluating 2Z is an intuitive shift. Booth encoding at higher orbits is achievable but for multipliers containing fewer than 32 bits, it doesn't appear to be worth building the other hard multiples. The fundamental structure of the Booth multiplier is displayed in Figure 2.

2.4. Conventional multiplier

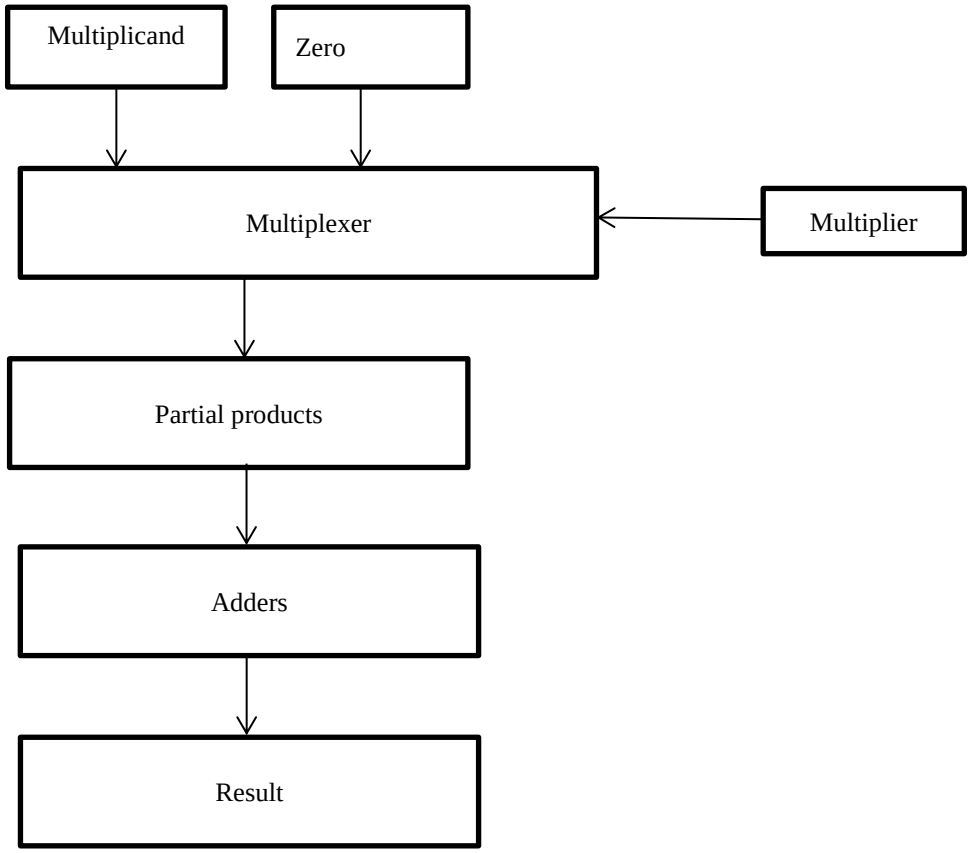

Figure 3. Block diagram of conventional multiplier

The N number of partial outcomes will be generated through a conventional multiplier of dimension N x N bits. Through bit-wise ANDing one multiplier bit alongside an additional multiplier, the partial products are created. As an outcome, the N x N bit multiplier utilizes N-adders and 2N-multiplications in the conventional multiplier design. The fundamental structure of a conventional multiplier is illustrated in Figure 3 above. When applying a Vedic multiplier, the additions and multiplications are considerably fewer than when utilizing a Booth or typical multiplier. Table 4 summarizes the hardware resources that were utilized, encompassing additions and multiplications for Vedic, booth, and conventional multipliers for 8x8-bit, 16x16-bit, and 32x32-bit processors.

Table 4. Total of addition and multiplications in multipliers

Multiplier Unit	**8x8- bit**	**16x16-bit**	**32x32-bit**
Conventional	65-Multiply 57-Add	257-Multiply 241-Add	1025-Multiply 1033-Add
Booth	41-Multiply 27-Add	97-Multiply 73-Add	289-Multiply 244-Add
Vedic	9-Multiply 5-Add	17-Multiply 9-Add	33-Multiply 17-Add

In Table 4, the initials "M" and "A" denote the multiplications and claims that consequently, were used across every width of the multipliers. Table 4 illustrates the explicit how Vedic mathematics will cut down the quantity of arithmetic and multiplier in contrast to the Booth and standard multipliers. The speed of the MAC unit increases as a consequence of the particular circuit's delay being reduced since we lessen the number of adder functions in each bit.

A superb multiplier ought to give an item that has been more modified, is easier to store, and consumes fewer resources. In this research work, we unveil an efficient high-speed zone Multiply and Accumulate unit (MAC) for 8-bit, 16-bit, and 32-bit measurements, based around the Vedic multiplication sutra architecture.

3. MULTIPLY ACCUMULATE UNIT:

Multiplication In immediate-time digital signal processing (DSP), aggregation performs an integral part in image processing and digital filtering, amid different uses. A fairly prevalent basic-level procedure involved in many DSP designs and algorithms is multiply and accumulate.

Immediately following doubling by two, the outputs are added to an aggregator register. The primary MAC unit has components made up of an accumulator, multiplier, and adder, illustrated in Figure 4. The standard multiplier unit entails multiplying the multiplier and multiplicand through the total number of the partial products that are created, and then figuring out the outcome of the multiplication. Usually, the MAC unit utilizes this. Therefore, as a result, the partial products are appended.

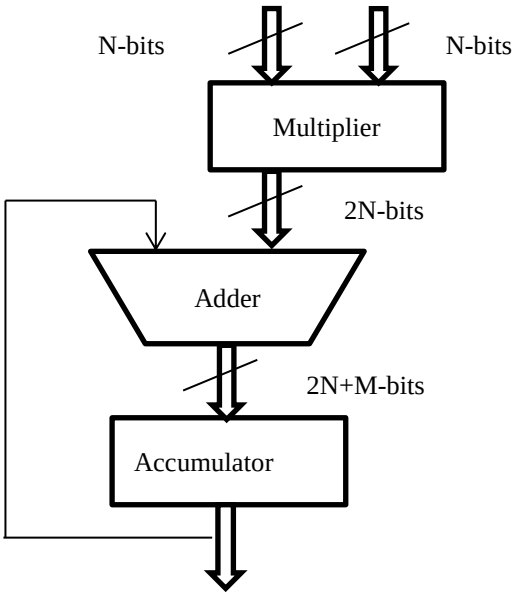

Figure 4. Structure of MAC Unit

Results

The approach is planned for 32-bit input employing Verilog-HDL. Modeling takes place implementing Xilinx ISE 12.3. Xilinx, Device Family: Spartan 3, Device: XCS100e, Package: tq144, Speed grade: -5, is applied for synthesis and execution. The entire system is finished of LUTs and multiplexers.

Table 5. Comparison of combinational path delay

Bit width dimension	Interruption of vedic multiplier	Interruption of proposed MAC
16-bit	23.645	11.324
32-bit	35.76	15.70

The combinational journey delay of the offered MAC module as well as the optimized Vedic multiplier discussed is evaluated in Table 5. It should be noted that the gate waits for the 16- and 32-bit demonstrated MAC modules are 11.324 ns and 15.69 ns, respectively, whereas the comparable optimized Vedic multiplier, has gate delays of 23.715 ns and 36.87 ns.

Figure 5 presents a speed comparison of the N-bit MAC unit along with outcomes for the 8-bit, 16-bit, and 32-bit MAC units. It is evident from Figure 5 that the latency increases with the number of bits. Figure 6 examines the size of an N-bit MAC unit and exhibits its results for an 8-bit, 16-bit, and 32-bit MAC unit. It might be seen that the area used advances with the number of bits.

Table 6. Comparison of synthesis analysis

MAC Unit	8-bit	16-bit	32-bit
Delay	7.839 ns	11.324 ns	15.69 ns
Amount of slices	45 out of 961 5%	95 out of 961 10 %	204 out of 961 22%
Amount of LUTs	70 out of 1921 4%	140 out of 1921 8%	314 out of 1921 17%

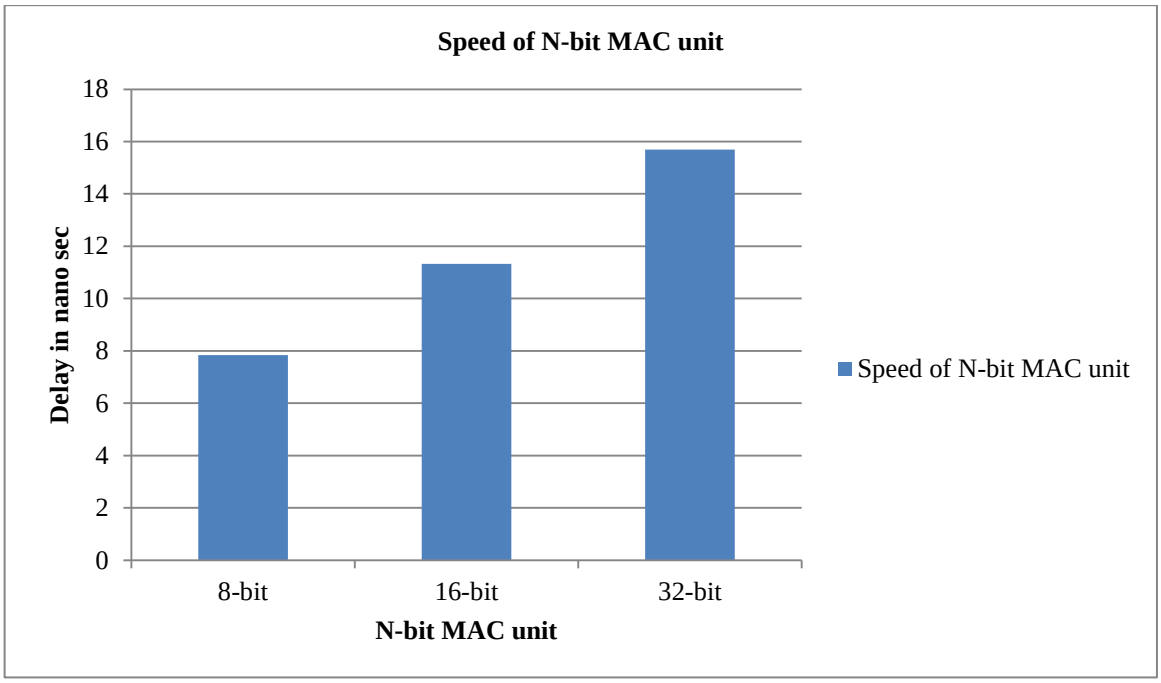

Figure 5. Speed of N-bit MAC Unit

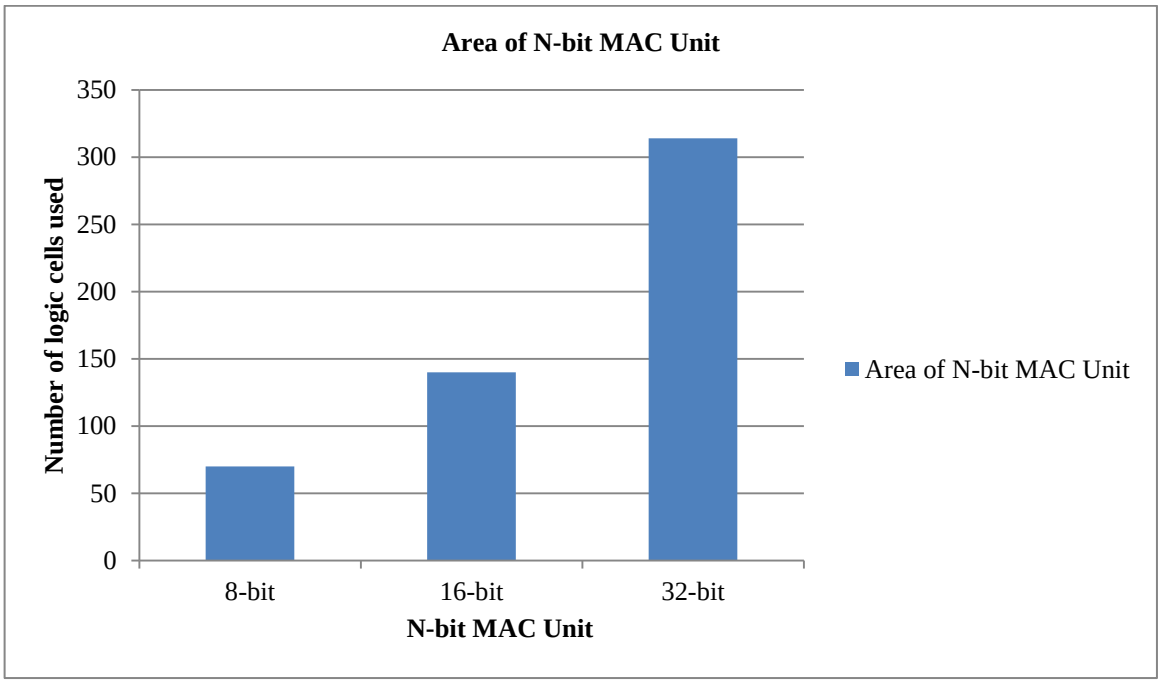

Figure 6: Area of N-bit MAC Unit

The juxtaposition of the computation outputs for the 8-bit, 16-bit, and 32-bit MAC layout is shown in Table 6. With roughly 3 percent device consumption (the total number of portions: 45 out of 961 5% and number of 4 input LUTs: 70 out of 1921 4%), the architecture's gate latency situations for 8-bit MAC is 7.839 ns. With almost 8% device utilization (number of slices: 95 out of 961, or 10%, and number of 4 input LUTs: 140 out of 1921, or 8%), the architecture's gate delay for 16-bit MAC is 11.324 ns. With a roughly 8% device utilization for 32-bit MAC, the architecture's gate delay is 15.69 ns (number of slices: 204 out of 961, or 22%, and number of 4 input LUTs: 314 out of 1921, or 17%).

The juxtaposition among Vedic MAC and standard MAC with in terms of area and tardiness is illustrated by outcomes of simulation and synthesis. It will be shown with a bar graph. The bar graph that ensues exhibits an approximate decline in both area and delay, revealing that Vedic MAC operates better

overall than regular MAC.

In microprocessors along with DSP applications, speed and chip size are significant factors, therefore the MAC will be tweaked for optimum throughput in a specific region. The pipeline technique is a common approach for improving digital circuit performance. We deploy pipelined architecture to increase multiplication and accomplish our maximum throughput aim [19].

4. CONCLUSION

In this paper we will discuss the techniques of multipliers and accumulators, which are the most important components in digital signal processing. We review several MAC architectures and discuss their effectiveness. Architectures developed at the transistor level show significantly better results than those developed at the HDL. Using a standard format such as IEEE 754 will improve the design process.

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