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Performance Comparison of CMOS and FinFET based Novel 9T SRAM Bit Cell

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Abstract: This paper aims to analyze and compare the parameters of a CMOS 90nm technology and FinFET with gate length 18nm, based 9T SRAM Bit Cell. These circuits are implemented to study the characteristics such as voltage transfer characteristics, delay, area and power consumption. Furthermore, in the case of FinFET SRAM cell, power consumption has been reduced by 39.4% with less propagation delay and 18% faster for read/write operations as compared to the CMOS technology. Also the read and write operations of the proposed SRAM cell are completely isolated from each other i.e. either read or write operation will be performed at a time.

Keywords: High speed, low power, FinFET, low power consumption, 9T SRAM cell.

1. INTRODUCTION

The Moore's law states that the number of transistors on a microchip doubles every two years, though the cost of computers is halved. However, there are certain limitations faced due to the existing technology of IC's. In the nanometre range, power dissipation is an important issue. Thus to achieve miniaturization, present MOS technology is not supported as the scaling reached the limit. So the alternative structures called FinFETs are to be substituted for the present circuits.

Over the deacdes, there has been a thrilling increase in the computing power and it has been possible due to the drastic advancements in the silicon integrated circuit (IC) technology which has been possible due to continuous miniaturization of the MOS transistor. The rapid improvements in circuit performance, its functionality and also the reduction in the manufacturing costs have collectively driven the semiconductor industry. The technique of scaling is the major driving force behind this progress. The speed of the circuit and the density has improved, due to reduction in dimensions of the physical MOS device, in the following ways: a) The operational frequency of the circuit increases when the corresponding gate length is reduced which is responsible for faster circuits. b) The chip area of the IC decreases which enables high transistor density resulting to cheaper ICs. c) A constant switching power density which allows a low power per function and hence the same power supports more circuits. Physical Limits are being reached for device scaling which used to be a straight forward affair till now and hence to continue the trends of scaling, new materials and device structures are required.

In the present world, the demand for laptops, cell phones etc. which are high speed and battery operated devices are increasing everyday. Primary memory is required which fast responses is required for the portable devices. To fulfil that purpose, a Static Random Access Memory (SRAM) is used which is significantly faster and doesn't require any refreshing. Due to the better performance property, the SRAM is always preferred over the Dynamic Random Access Memory (DRAM) but unlike the DRAM, SRAM cell requires continuous supply voltage to retain the stored data and hence it consumes more power.

Some of the highlighting issues of high speed Static RAM cells are dynamic power dissipation and leakage current where it contributes to total power consumption, in large parts, which is responsible for the reduction in the battery life of the devices these are used in. Thus an efficient design of an SRAM cell is required which has low delay, high speed, low power consumption.

Hence in this paper, CMOS and FinFET based 9T SRAM cell is implemented and the various parameters are analysed and hence comparison is done between the two technologies.

2. THE FINFET TECHNOLOGY

The FinFET devices significantly subdue the short channel effects, lower energy and power suppression,

International Innovative Research Journal of Engineering and Technology
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high supply voltage scaling capability compared to the bulk CMOS. The most notable attributes of the FinFET are:

a) Reduction in short-channel effects due to ultra-thin silicon fin.

b) Reduction in parasitic resistance due to an uplifted source and drain which is covered by the gate electrode.

c) Increase in the drive current.

d) Multiple fins are used by FinFETs to attain larger channel widths.

A schematic representation of the FinFET Technology has been shown in Fig. 1. Due to the fact that channel width of FinFET is perpendicular to its surface thus by varying the fin height, the on current and channel width is increased. The static power dissipation is overcome by the FinFET transistors by controlling the channel potential by wrapping the fin around the two gates [1]. The low poer area efficiency of FinFETs are useful as it replaces the two parallel transistors with one only if the transistor's gate signals are applied to its two independent gates.

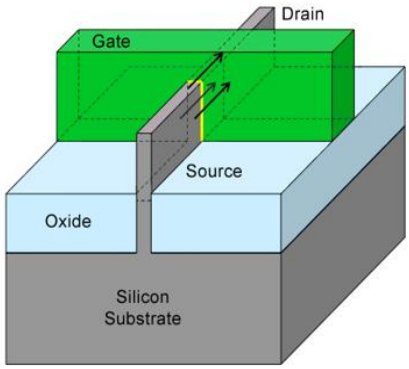

Figure 1. A Schematic representation of the FinFET Technology

3. PROPOSED 9T SRAM CELL USING CMOS TECHNOLOGY

In this section, we propose the schematic diagram of the proposed 9T SRAM using the CMOS 90nm Technology. Here, the transistors NM4 and NM5 are access transistors with W/L ratio of 0.85, which are responsible for controlling the connection between the Bit lines B and BB. The novelty of the proposed 9T SRAM being that this configuration has separated and isolated Word line and Read line named as WBL and RBL respectively. The functional analysis of the proposed 9T SRAM Cell has been presented sequentially as: (i) write; (ii) read;

The write operation takes place by enabling write bit-line (WBL). During the write operation, the transistors NM2 and NM6 only allows a small leakage current due to the fact that the transistor NM6 is in the cut-off state. This is called the Super cut-off CMOS (SCCMOS) Technique. By increasing the width to length (W/L) ratio of the transistors NM2 and NM3 [2], the Static Noise Margin is improved.

A differential read operation is employed by this configuration for the better read access time and hence a symmetrical design has to be made for this purpose. At the beginning of the read cycle, the RBL is activated and the transistors NM2 and NM3 are switched ON thus forming a stronger pull down circuit. The circuit diagram for the proposed 9T SRAM cell using CMOS technology has been shown in Fig.2.

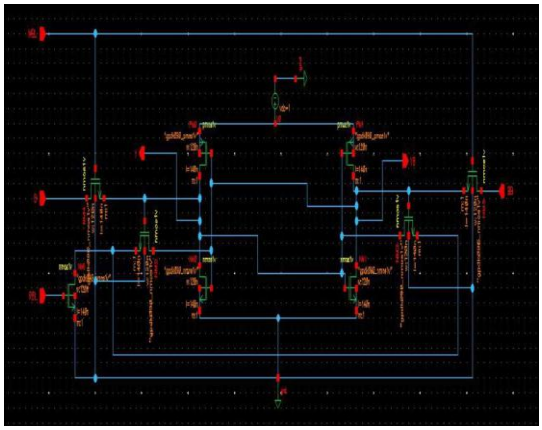

Figure 2. The proposed CMOS Based 9T SRAM Cell

4. PROPOSED 9T SRAM CELL USING FINFET TECHNOLOGY

In this section, the schematic diagram of the proposed 9T SRAM using the FinFET Technology with gate length of 18nm is shown. It has been designed for the purpose of improved scalability [3,4], the FinFET design is good for the memory applications. It is designed as such to overcome much of the technology concerns in a typical planar device. In turn, this generally lessens many constraints of the SRAM devices. The short channel effects are suppressed by the FinFET's thin body and hence light doping can be done for the body channel which minimizes the threshold voltage variations [5]. The transverse electric field is reduced and hence minimization of carrier mobility and impurity scattering is possible. The depletion charge along with the capacitance is reduced which is responsible for reduced leakages and steep sub-threshold. The bitline loading is is reduced due to the lower capacitance in these FinFET

International Innovative Research Journal of Engineering and Technology
ISSN: 2456-1983 Vol: 5 Issue: 3 March 2020

devices and hence improves SRAM performance. Thus, it is found that the FinFET devices have increased performance improvements over CMOS devices as technology scales.

FinFETs have namely three methods of activity i.e. hamper, low, power mode and autonomous door mode [6]. The transistor design is of shorted door (SG) and is illustrated in Fig. 3(a). In the low-control (LP) working mode, exhibited in figure 3(b), on which the use of turn around predisposition on the back door reduces the spillage current significantly. The back door can be fixing to another info, prompting autonomous entryway (IG) working mode, illustrated in fig.3(c).

The CMOS configuration is modified to FinFET technology with two p-fins and seven n-fins. The gate drawn length for all the FinFETs are kept same which is 18nm and poly MOS length is 48nm. The number of fins used per finger is 1 for both n-fins and p-fins where number of fingers are set to 1.Excess n-fins are used to control bit lines and inputs for memory block. Four separate clock pulses are used as an input for read, write, bit and bitbar lines.

The circuit diagram for the proposed 9T SRAM cell using FinFET technology has been shown in Fig.4.

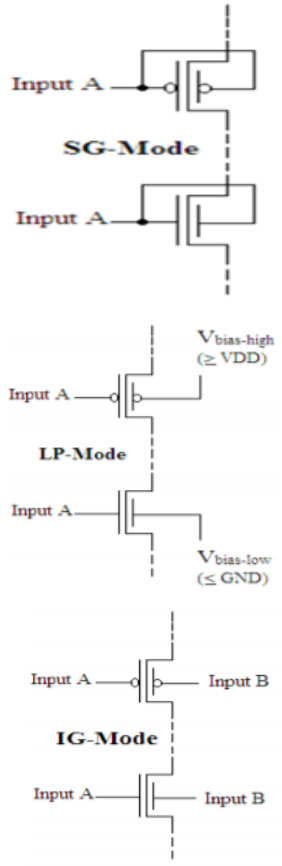

Figure 3. (a) Shorted-gate (SG) mode Fig. 3(b) Low-power (LP) mode Fig. 3(c) Independent-gate (IG) mode

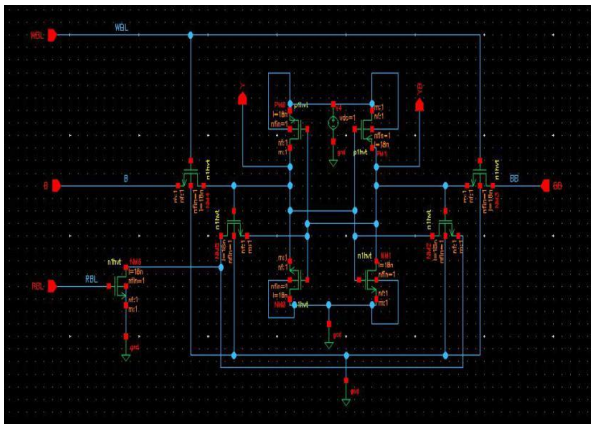

Figure 4. The proposed FinFET Based 9T SRAM Cell

5. SIMULATION RESULTS AND ANALYSIS

This section aims to present the output curves of the simulations of both the technologies i.e. CMOS and FinFET. The output curves have been shown for the parameters such as transient response, power analysis, Static Noise Margin and delay. Same testing conditions of parameters for both the technologies has been employed for the simulations to ensure the uniformity, accuracy and precision in the analysis of both the designs. The simulations are presented as follows:

5.1 Simulations for the CMOS based SRAM Cell

5.1.1 Transient Response/ Timing Diagram

(a) Write Operation

When the write bit line (WBL) is active, the binary data available on bit line is fed into memory block of SRAM Cell. This WBL pulse enables the two access transistors which are connected to the bit lines. From the transient response we can see that when the writing pulse is active to 1 and bit line is carrying binary 1, output is successfully written to 1.

(b) Read Operation

When the read pulse (RBL) is active, the binary data stored in the memory block is read from it.The output for this operation will come out to be same as the stored bit. From the transient response we can see that when read pulse is active to 1, the output pin shows the previously stored bit i.e., 1 from the memory block. Both read and write operations are isolated from each other.Hence, only one operation can be done at a time.

International Innovative Research Journal of Engineering and Technology
ISSN: 2456-1983 Vol: 5 Issue: 3 March 2020

The transient response obtained via simulation has been shown in Fig. 5.

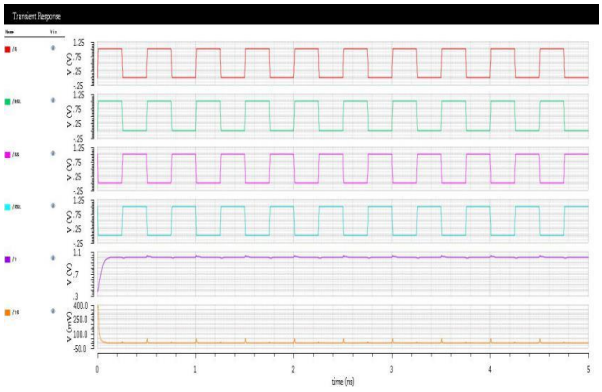

Figure 5. Transient Response/ Timing Diagram for 9T SRAM Cell (CMOS)

5.1.2 Power Analysis

When the circuit is switched ON and initial operations are done, then the maximum power consumption can be seen in the graph which is indicated by the highest peak. The following consecutive peaks shows the power consumption during switching between read and write operations. But both of these consume the same amount of power when operated separately. The power analysis simulation result has been shown in Fig. 6.

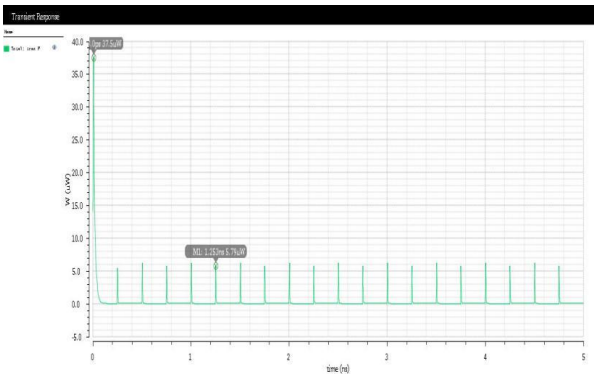

Figure 6. Power Analysis for 9T SRAM Cell (CMOS)

5.1.3 Static Noise Margin

To obtain the SNM characteristics, a butterfly curve is to be plotted at first. For obtaining the butterfly curve, the feedback circuit of the cross-coupled inverter configuration is separated. After that, DC analysis is performed at node Y and node YB. The butterfly curve is plotted by toggling the axis of one of the VTC curves, and merging the two separate VTC graphs together**.** SNM of the SRAM cell relies on the cell ratio (CR), DC voltage applied and pull up ratio. For stability of the SRAM cell, high SNM is required that depends on the value of the cell ratio, pull up ratio and DC voltage applied to the circuit. Generally, to improve the SNM, the threshold values of the NMOS and PMOS devices has to be increased. However, the increment in threshold values of PMOS and NMOS devices is limited. The reason being that the SRAM cells with MOS devices having too high threshold values are difficult to operate as well as it is hard to flip the operation of MOS devices. The butterfly curve obtained has been shown in Fig. 7.

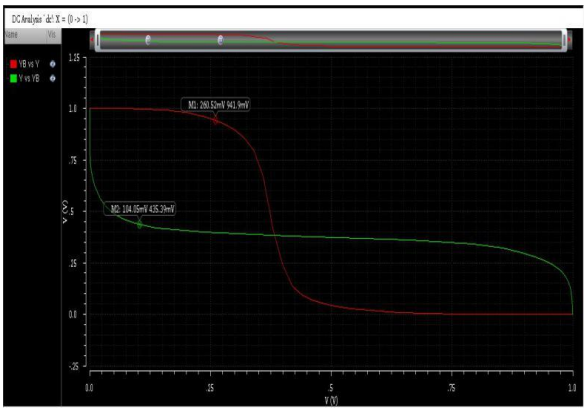

Figure 7. Butterfly curve for SNM for 9T SRAM Cell (CMOS)

5.1.4 Propagation delay

The delay for the circuit can be calculated from the timing diagram. The initial delay for the output to reach its maximum voltage is in range of picoseconds (ps) which clearly can be seen when the WBLbecomes active and Bit line set to 1.Small consecutive dips similarly shows the delays for switching between read write operations. The visual representation of the delay in the output is shown in Fig. 5.

5.2 Simulations for the FinFET based SRAM Cell

5.1.1 Transient Response/ Timing Diagram

(a) Read Operation

When the read bitline (RBL) is active, the binary data stored in the memory is read from it. The output for thi operation will come out to be same as that of the stored bit. From the transient response we can see that when read pulse is active, the output shows the previously stored bit i.e. 1 from the memory block. Both read and write operations are isolated from each other. Hence, only one operation is performed at a time.

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(b) Write Operation

When the write bitline (WBL) is active, the binary data available on bit line is fed into the memory block of SRAM cell. This WBL pulse enable the two access transistors which are connected to the bitlines. From the transient response we can see that when the writing pulse is active to 1 and bitline is carrying binary 1, output is successfully written to 1. The transient response obtained via simulation has been shown in Fig. 8.

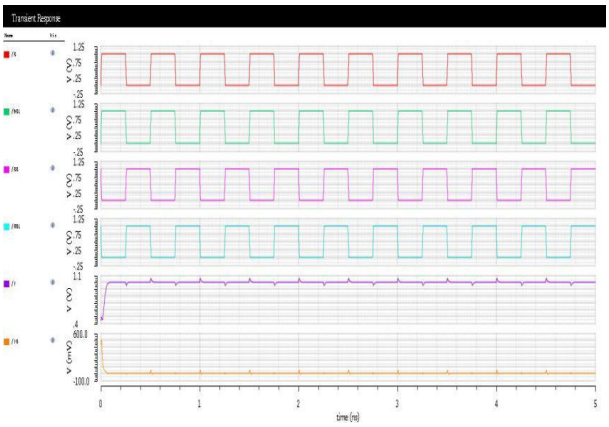

Figure 8. Transient Response/ Timing Diagram for 9T SRAM Cell (FinFET)

5.1.2 Power Analysis

When the circuit is switched ON and initial operations are done, then the maximum power consumption can be seen in the graph which is indicated by the highest peak. The following consecutive peaks shows the power consumption during switching between read and write operations. But both of these consume the same amount of power when operated separately. The power analysis simulation result has been shown in Fig. 9.

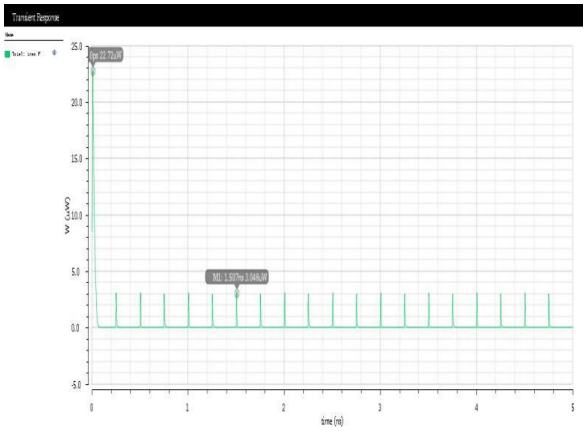

Figure 9. Power Analysis for 9T SRAM Cell (FinFET)

5.1.3 Static Noise Margin

To obtain the SNM characteristics, a butterfly curve is to be plotted at first. For obtaining the butterfly curve, the feedback circuit of the cross-coupled inverter configuration is separated. Following this, the DC analysis is performed at node Y and node YB. Butterfly curve is plotted by toggling the axis of one of the VTC curves, and merging the two separate VTC graphs together**.** SNM of the SRAM cell relies on the cell ratio (CR), DC voltage applied and pull up ratio. For stability of the SRAM cell, high SNM is required that depends on the value of the cell ratio, pull up ratio and dc voltage applied to the circuit. In order to improve the SNM, the threshold values of the NMOS and PMOS devices has to be increased. However, the increment in threshold values of PMOS and NMOS devices is limited. The reason being that SRAM cells with MOS devices having too high threshold values are difficult to operate as well as it is hard to flip the operation of MOS devices. The butterfly curve obtained has been shown in Fig. 10.

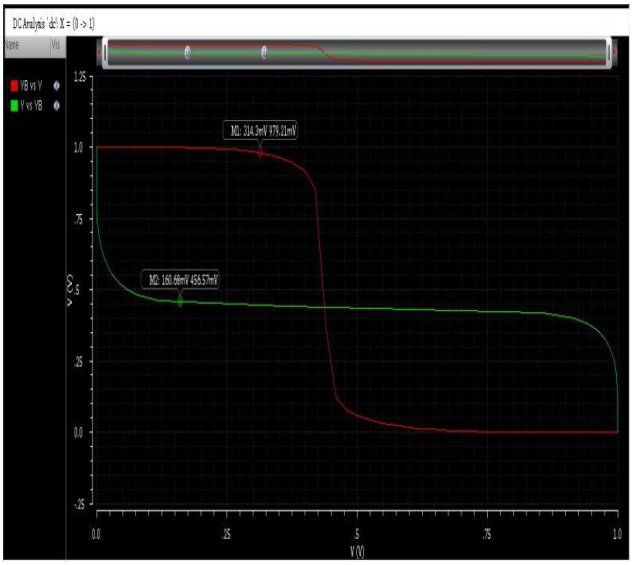

Figure 10. Power Analysis for 9T SRAM Cell (FinFET**)**

5.1.4 Propagation delay

The delay for the circuit can be calculated from the timing diagram. The initial delay for the output to reach its maximum voltages is in range of picoseconds which clearly can be seen when the WBL becomes active and bitline is set to 1. Small consecutive dips show the delays for the switching between read and write operations.

5.1.5 Relationship between the Number of Fins, Delay and Power Consumption

The fin in the FinFET carries majority charge carriers which contributes to drain current and output voltages. These fins connect the source and drain terminal that is wrapped around polysilicon gate layer. The majority charge carriers increases as the number of fins increases which in turn increases the drain current and hence reduces the delay. But these extra fins make the circuit to draw more power from the source to supply sufficient majority charges. Hence, the reduction in delay comes at a cost of increased power consumption. The Table 1 gives the comparison between the number of fins increasing consecutively and the power consumed during switching and the maximum power consumed. The quantitative representation for this is shown in Table 1.

Table 1. Relationship between the number of fins, Delay and Power Consumption

Number of Fins	Delay	Max. Power Consumed	Power consumed during switching
1	45.2 ps	22.72 μW	3.04 μW
2	32.9 ps	42.51 μW	5.53 μW
3	28.6 ps	62.11 μW	8.043 μW
4	26.7 ps	81.64 μW	10.25 μW
5	25.6 ps	101.1 μW	13.48 μW

6. PARAMETRIC COMPARISON BETWEEN CMOS AND FINFET BASED 9T SRAM CELL

This section provides the comparison between the CMOS and FinFET based configuration of the proposed 9T SRAM Cell based on several parameters such as the maximum power consumption in a single iteration, power consumption during switching between read and write operations, static noise margin, delay, speed. The juxtaposition between the CMOS and FinFET based configurations based on the various parameters is shown in Table 2.

Table 2. Comparison of CMOS and FinFET Configurations based on various parameters

Parameters	9T SRAM (CMOS)	9T SRAM (FinFET)
Maximum Power Consumption	37.5 μW	22.72 μW
Power Consumption during Switching	5.79 μW	3.04 μW
Static Noise Margin	374.82 mW	384.72 mW
Delay	54.9 ps	45.2 ps
Speed	-	18% Faster

7. CONCLUSION

A novel 9T SRAM cell using CMOS with 90nm technology and FinFET of gate length 18nm technology has been implemented with high switching speed, reduced delay and reduced power consumption. The operations of read and write are completely isolated from each other and both the operations occurring once at a time and not simultaneously. The proposed configurations have also achieved high SNM and reduced delay for which the FinFET configuration showed better results over the standard CMOS configuration. This has been justified in the parametric comparison between the two technologies. Hence, the power consumption for FinFET technology has been reduced by 39.4% with an 18% increment in speed compared to the CMOS technology.

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